LASER SYNCHRONIZATION AT REGAE USING PHASE DETECTION AT AN INTERMEDIATE FREQUENCY

M. Felber#, M. Hoffmann, U. Mavric, H. Schlarb, S. Schulz, DESY, Hamburg, Germany
Wojciech Jalmuzna, TUL-DMCS, Lodz, Poland

Abstract

At DESY in Hamburg a new linear accelerator is being set up for electron diffraction experiments. This machine, called REGAE (Relativistic Electron Gun for Atomic Exploration), is composed of a photo-cathode gun and a buncher cavity. It uses one laser system for both the generation of the electron bunches and for pump-probe experiments. At the experiment the required timing jitter between the electron bunches and the laser pulses is in the order of 10 fs. The conventional method for laser synchronization using RF technique to measure phase(jitter) in the baseband is susceptible to distortions caused by ground-loops and electro-magnetic interference. At REGAE a new scheme for an RF-based laser synchronization is deployed. It uses a down-converter which mixes a higher harmonic of the laser repetition rate down to an intermediate frequency (IF). The IF is digitized and its phase is calculated. This information is used for the feedback controller to keep the laser synchronized to the RF reference.

THE REGAE FACILITY

REGAE is a joint project of the CFEL partners Max Planck Society, University of Hamburg and DESY. The linac is approximately ten meters long and generates highly coherent ultra-short (10 fs) electron pulses to carry out time resolved structural investigations of crystallized materials by femtosecond electron diffraction and possibly push the boundaries to in situ studies of liquids, surface and solution phase chemistry on the nano-scale [1]. In order to meet the requirements of high electron densities and short bunches for these kind of experiments, space charge effects have to be overcome by using relativistic electron bunches with charge well below 1 pC. The transverse coherence length should be in the order of 30 nm [2, 3].

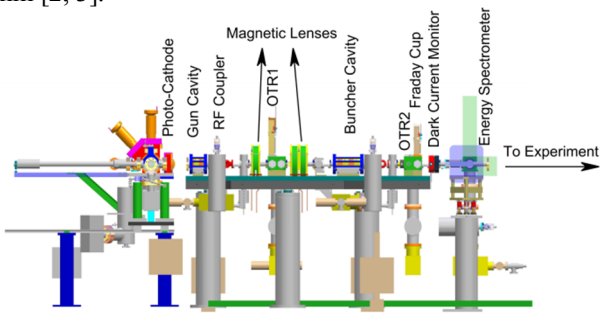

Figure 1: Layout of the REGAE linac.

The bunches are generated by shooting the third harmonic (265 nm) of a commercial Ti:sapphire laser on a Cs_2Te photo-cathode inside the RF gun which accelerates the electrons to 2-5 MeV. After focusing and collimation by solenoid magnets a buncher cavity ballistically compresses the bunches to about 10 fs at the sample target where pump-probe experiments are carried out with the same laser source which is used for the cathode. Numerous low-charge single shot electron diagnostic measurements like emittance, energy, energy spread and bunch length are mandatory to produce and maintain the quality of the beam [4]. The machine layout is shown in Figure 1.

RF SYSTEM AND TIMING

REGAE operates with a maximum repetition rate of 50 Hz and the duration of RF pulses is 6 us. The 1½-cell gun and 4-cell buncher cavities are normal-conducting S-band structures powered by one klystron.

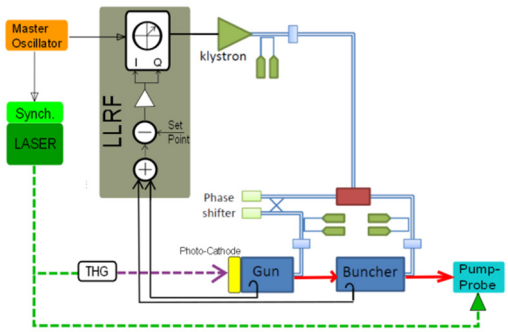

Figure 2: Block diagram of the RF system with the laser.

The arrival-time jitter between electron bunch and laser pulse at the target is determined by both the stability of the accelerating field and the synchronization of the laser. For achieving values in the 10 fs range, the field must be stabilized to 0.01% in amplitude and 0.01 degrees (at f_{RF} = 3 GHz) in phase by the Low-Level Radio Frequency (LLRF) control. The vector sum of both cavities is calculated from probe signals which are sampled with 125 MSPS after down-conversion. The digital controller acts on a vector modulator modulating the 3 GHz reference from the master oscillator to drive the high power RF chain (see Figure 2). Feedback and learning feed-forward algorithms are foreseen.

In order to avoid 50 Hz distortions from the mains in power supplies, the machine trigger is always shifted as close as possible to the zero crossing of the 50 Hz. This is realized within a master timing module which then delivers the trigger for the LLRF, the high power RF, the diagnostic tools, and for the amplifier system of the laser. The trigger has to be synchronous to the continuous machine frequencies from the master oscillator and the

matthias.felber@desy.de

laser repetition rate. To achieve this, a base frequency (f_B) whose zero crossing lines up with all other zero crossings is generated and the trigger is shifted in steps of periods of f_B. In this case, 1 kHz is taken as f_B because it is the lowest frequency in the system [5]. Table 1 is listing the values of most relevant frequencies at REGAE.

Table 1: REGAE frequencies

Main RF (f_{RF})	2.9979 GHz
LO for down-converter (f_{LO})	3.0229 GHz
IF from down-converter (f_{IF})	24.983 MHz
ADC clock (f_s)	124.91 MHz
Reference input timing (f_t)	0.9993 GHz
Laser oscillator rep. rate ($f_{Ti:Sa}$)	83.275 MHz
Laser amplifier rep. rate (f_{las}=f_B)	1.0009 kHz

µTCA HARDWARE PLATFORM

At DESY REGAE is the first facility whose operation and control relies on the new hardware platform µTCA (micro Telecommunications Computing Architecture) which was chosen for the European XFEL to replace the commonly used Versa Module Eurocard (VME) system. The new industry standard MTCA.4 for delicate I/O requirements assures the quality of analog signal processing [6].

Advantages of the new standard include faster data processing of more channels, full remote management, hot-swap capabilities, redundant architecture, a more compact design, reliability, and modularity. The hardware is composed of double sized Advanced Mezzanine Card (AMC) modules with optional Rear Transition Modules (µRTM) e.g. for analog I/O connections.

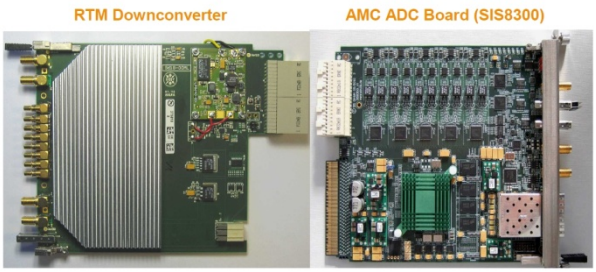

Figure 3: Hardware used for laser synchronization.

At REGAE the LLRF and the timing use the new platform, making it beneficial for both sides: for the firmware developments it offers the possibility for field application testing and debugging and for the facility it offers much better possibilities for control architecture. The new scheme for laser synchronization at REGAE which is presented in this paper relies on the same hardware infrastructure like the LLRF control [7]. It is composed of a µRTM (Figure 3, left) housing analog input channels with down-converters to generate an intermediate frequency and a front AMC (Figure 3, right) where the IF is digitized by fast ADCs and processed in a Xilinx Virtex 5 FPGA [8].

SYNCHRONIZATION SETUP

The Ti:sapphire laser oscillator ("Micra-5" from Coherent®) has a repetition rate of about 83 MHz with an average power of 350-400 mW at 800±30 nm. A fraction (< 10%) of the free-space beam guided from the oscillator to the amplifier is split, separated, and sent to two GaAs photo diodes of 10 GHz bandwidth. Beforehand the beam is sent through a so-called noise eater which is a low-bandwidth amplitude stabilizer to avoid artificial phase drifts due to the amplitude-to-phase conversion effect in the diodes. The 36th harmonic of the pulse repetition rate, which is ~3 GHz like f_{RF}, is extracted from the spectrum of both diodes with band pass filters and amplified to about 5 dBm each.

One of these signals is transported via ~10 m coaxial cable to the µTCA crate housing the afore mentioned controller hardware. To minimize phase drifts during transmission low-drift 3/8" heliax cables are used [9]. The signal is fed from the rear to the down-converter µRTM where the IF is generated. After transmission to the front AMC it is digitized and further processed by the controller firmware whose simplified block diagram is shown in Figure 4.

The second 3 GHz signal which is gained from the laser oscillator is used for a back-up setup providing rudimentary laser synchronization in case the new scheme is not available e.g. due to maintenance or development work. This setup uses the conventional method of down-mixing to baseband in a double-balanced mixer with the help of the 3 GHz reference from the master oscillator. This kind of scheme is well known and applied at different locations in FLASH as part of the optical synchronization system [10]. The feedback is performed by an analog proportional-integral controller.

Both, the back-up analog and the digital FPGA control result in a baseband voltage which is amplified by an in-house-built piezo driver. The driver output acts on a piezo within the laser cavity changing frequency and phase of the optical pulse train in order to synchronize it to the reference. The laser also incorporates a stepper motor for coarse tuning.

FPGA SIGNAL PROCESSING CHAIN

The digital down-conversion of the IF to baseband in the FPGA is carried out with a classical quadrature detector (Figure 4). A moving average filter (over 5 samples) is used for proper filtering before decimating the data by 100. The bandwidth reduction simplifies the design of the following processing stages and gives extra protection for the piezo driver. A matrix rotator used as a phase shifter which is acting on the detected I and Q signals allows for proper phase alignment once the laser is locked to the RF. A classical implementation of the CORDIC [11] algorithm allows calculating the amplitude and the phase of the detected signal.

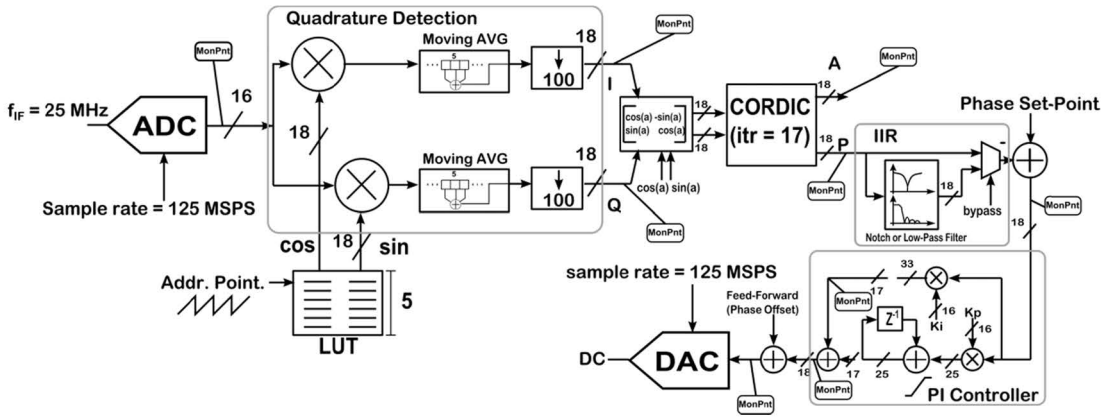

Figure 4: Building blocks of the firmware for digital phase detection and feedback algorithms realized in the Virtex 5 FPGA on the ADC AMC module "SIS8300" from Struck GmbH [8].

The measured phase is passed through an IIR structure that can be configured as a notch filter or as a low-pass (LP) filter. The notch filter is used for suppressing the self-resonance of the piezo, which is about 50 kHz in this case. The LP filter is used if a general reduction of the open-loop bandwidth is desired. The filtered signal is subtracted from a set-point value (normally 0) and routed to a proportional-integral controller. The output of the controller is added to an offset value which is defined by the user. The offset is used as a feed-forward signal that sets the coarse position of the piezo before adding the output of the fast controller. The platform provides several debug and monitoring signals that are read through the PCIe bus. Up to now a Matlab-based graphical interface is used for controlling parameters of the firmware.

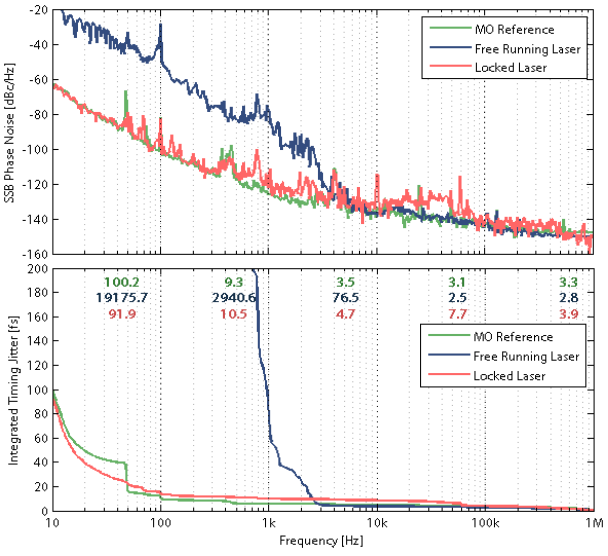

Figure 5: Phase noise and integrated timing jitter of the 3 GHz reference, the free running-, and the synchronized laser. The numbers in the lower plot represent the jitter in the individual frequency decades in femto-seconds.

FIRST RESULTS

The presented system is still in a development state (May 2012) whose lack of automation prevents it from being used continuously. Nevertheless, very promising results have been achieved in terms of residual jitter between the laser pulse train and the 3 GHz master reference. The synchronization is in the order of 10-20 fs (Figure 5) which is about 4 times better than could be achieved with the analog setup and control.

Another big advantage compared to the traditional scheme with analog mixer is that the use of a vector modulator as phase shifter is no longer needed because the phase is simply set in software.

CONCLUSION AND OUTLOOK

The commissioning of REGAE is progressing; within the year 2012 pump-probe experiments and jitter measurements between electrons and laser are planned.

The implementation of the new scheme for laser locking is showing excellent results. It offers high flexibility e.g. for filter implementation and makes larger analog RF setups which are very susceptible to drifts and electric distortions obsolete. It has already being adapted to the new injector laser at the Free-Electron Laser FLASH and is foreseen for other systems as well.

Next steps are server development for automation and implementation to the control system including a 83 MHz bucket detection and laser coarse motor tuning.

REFERENCES

[1] http://www.desy.de/news/@@news-view?id=1701
[2] M. Hada et al., JT2A.47, ICUSD2012
[3] K. Floettmann, DESY Annual Report 2011, p. 34 http://www.desy.de/sites2009/site_www-desy/content/e410/e84441/e107152/Accelerators_2011_ger.pdf
[4] Sh. Bayesteh et al., TUPC081, IPAC2011
[5] M. Felber, internal White Paper, http://ttfinfo.desy.de/REGAEelog/index.jsp
[6] K. Rehlich, THA006, ICALEPCS2009.
[7] J. Branlard, MOOAC01, this conference
[8] http://www.struck.de/sis8300.html
[9] K. Czuba and D. Sikora, ACTA PHYSICA POLONICA A, 119, 553 (2011)
[10] M. Felber et al, THOA3, FEL2010.
[11] R. Andraka, proceedings of FPGA '98, p. 191